Dept. of Electrical Engineering, IIT Bombay 24th Feb 2017 GPS/IRNSS Receiver Signal Flow Graph Description Author: Chirag Shetty (chiragcshetty@gmail.com) Advisor: Prof. Madhav P. Desai

(Please refer to the signal flow graph diagram attached. The labellings (1) to (23) in the diagram are described in this document)

• ① Raw signal received at the antenna:

$$s_r(t) = \sqrt{2P} D(t - \tau) x(t - \tau) \cos(2\pi (f_c + f_d)t + \theta) + n(t)$$
where, $D(t) = Navigation Data Bits$
 $x(t) = PRN \ code$
 $\tau = Signal \ Travel \ Time$
 $f_c = Carrier \ Frequency$
 $f_d = Doppler \ Frequency \ Shift$
 $n(t) = White \ Gaussian \ Noise$

• 2) Amplified band-pass filtered signal about f_c :

 $s_r(t) = \sqrt{2P} D(t-\tau) x(t-\tau) \cos(2\pi (f_c + f_d)t + \theta)$ $+ n_I(t) \cos(2\pi f_c t) - n_Q(t) \sin(2\pi f_c t)$ $where, n_I(t) + jn_Q(t) = Baseband equivalent of the band-pass filtered white noise$

As per the ICD, maximum signal power received at the antenna (in 20MHz) is -153dbW (i.e 123dBm), and -139dB after LNA of 14dB. The noise power at antenna can be found as $N = kT_E B$, where k is the Boltzmann's constant (1.3806 × 10⁻²³ JK⁻¹), T_E kelvin is effective noise temperature (513K) and B is the concerned bandwidth (20MHz in this case). That gives noise density of -201.5 dBW/Hz and noise power of -201.5 + 73 = -128.5 dBW (-114.5dBW after LNA of 14dB). So maximum SNR that can be expected is -153 + 128.5 = -24.5 dB. (Ref: GPS Receiver Architectures and Measurements, Michael S. Braash, A. J. Van Dierendonck,)

• (3), (4) Signal downconverted to intermediate frequency f_i . Power entering LO is about (-114.5+20 = -95.5dBW). Output after low pass filtering (ignoring the $\sqrt{2P}$ term) is:

$$s_r(t) = D(t-\tau) x(t-\tau) \cos(2\pi (f_i + f_d)t + \theta)$$
$$+ n_I(t) \cos(2\pi f_i t) + n_Q(t) \sin(2\pi f_i t)$$

Power at ④ is about -95.5dBW - 3dB (loss in LO+LPF) + 20dB (RF Gain) = -78.5dBW. More RF gain stages may be required before the signal enters LO. As a thumbrule the input power in the frequency region of interest should be atleast 20dB above the noise floor at other frequencies after adding the noise figure of the LO. So we'll need a gain of atleast 20dB + (noise figure of LO) in the RF stage.

More IF gain stages may be required to ensure that the input (desired signal + noise) to ADC has enough dynamic range. Automatic Gain Control can be used at this stage to make the most of ADC's range. Also f_i should be chosen small enough to be within the analog bandwidth of the ADC.

• (5) The N-bit sampled signal. The sampling frequency F_s should be greater than twice the bandwidth considered (Nyquist Criterion). Sampling gives a copy of the input near baseband



Figure 1: Early-Late DLL

at $f_i - n \times F_s$ for some integer n. This frequency $f_i - n * F_s$ can be used in subsequent setups to bring the signal to baseband. The sampled signal is processed in packets of Tms where Tis 1 or 2 initially and is increased after a lock is achieved. Greater the T, better are detection probabilities but the search space in acquisition increases.

• (6), (7), (8) Acquisition: The sampled signal is corelated with locally generated C/A code and carrier. Frequency space is searched for a coarse estimate \hat{f}_d of the doppler shift f_d from f_i - 10kHz to f_i + 10kHz at intervals of 500/T Hz. Simultaneously, all code phases are searched to find an estimate $\hat{\tau}$ for τ . For a given $\hat{\tau}$ and \hat{f}_d the result of point-wise multiplication of samples and the locally generated replica can be represented as a complex number $D(t-\tau) x(t-\hat{\tau}) x(t-\tau) \exp(j2\pi(f_d - \hat{f}_d)t) \exp(j\theta)$ (neglecting the high frequency component).

The output at $(\widehat{b}, \widehat{c})$ is the sum of terms as mentioned above (i.e dot product of signal samples and local replicas). The output is the corelation function as defined below. Let $\Delta \tau = \tau - \hat{\tau}$ and $\Delta f_d = f_d - \hat{f}_d$

$$\tilde{S}(\Delta\tau, \Delta f_D, \theta) = D e^{j\theta} \underbrace{\int_0^T x(t-\tau)x(t-\hat{\tau}) \exp(j2\pi\Delta f_d t)dt}_{\tilde{R}(\Delta\tau, \Delta f_d)}$$

Where \tilde{S} is the co-relation function & \tilde{R} is called the ambiguity function. Thus output at \circledast is $\left|\tilde{R}\right|^2$ and is computed for all frequency and code-phase shifts. The peak will correspond to $\hat{\tau}$ and \hat{f}_d .

- (9) The acquisition of the satellite is flagged to be complete is either the peak value is large, which happens when the SNR is very good, or if the current estimates $\hat{\tau}$ and \hat{f}_d match the estimates of the previous acquisition step exactly. If both the conditions fail, acquaition is restarted with the next $F_s \times T$ samples, else tracking is initiated.
- (10)Tracking, Early-Late Detector: Before locking to the exact doppler shift using a PLL, the receiver must identify the exact code-phase. This is implemented using the Early-Late detector, where the difference in ambiguity function d code-shifts before and after $\hat{\tau}$ is added back as the feedback (modulo $F_s \times 1ms$). The feedback constant used is $\frac{1}{2F_s \times 10^{-3} \times T^2}$. This is so chosen that the DLL shifts by one chip if the maximum possible value of the feedback is achieved. The feedback refines $\hat{\tau}$ every T ms.
- (11)Tracking, FLL and PLL: Once the code phase is matched, the corelation function can be used to correct for the residual doppler offset. Once $\hat{\tau} = \tau$, we have:

$$\tilde{S}(\Delta f_d, \theta) = D e^{j\theta} \int_0^T \exp(j2\pi\Delta f_d t) dt$$
$$= D \frac{\sin(\pi\Delta f_d T)}{\pi\Delta f_d} e^{j(\theta + \pi\Delta f_d T)}$$

Clearly, $Arg[\tilde{S}(\Delta f_d, \theta)] = \theta + \pi \Delta f_d T$

From acquisition, $\Delta f_d \leq 500$ and T=1ms, thus $\pi \Delta f_d T \leq \frac{\pi}{2}$. When Δf_d is small, taking -1 as the feedback constant for θ corrects for the phase offset at once.

- (12) Clamp: The feedback $\theta + \pi \Delta f_d T$ can at times become large due to noise, and causes an ambiguity of π since *atan* discriminator is agnostic to π -shifts. Thus we clamp the feedback to $\pm \frac{\pi}{4}$.
- (13), (14), (15) Update steps: The code phase estimate, doppler estimate and phase offset are updated every Tms using appropriate wrapping condition (2π for phase, $F_s \times 10^{-3}$ for code-phase).
- (16) Tracking Lock indicator: A moving average of the phase error feedback is used for robust detection of locking. Error is fed to filter $1 + 0.9z^{-1}$ and the output is monitored. When it becomes less than a threshold (10 in the implementation, found experimentally), lock is declared. A drawback of this lock detector is that a sudden large error with declare loss of lock, and it takes sometime for it to settle back to less than threshold. However this can be taken care by the processor by waiting until for a programmed amount of time for it to re-lock.
- (17) Navigation Bits: As PLL proceeds, $\Delta f_d \rightarrow 0 \text{ or} \pi$, and the imaginary part of corelation function goes to zero and sign of the real part gives the data bit D with an constant ambiguity of ± 1 .

$$\lim_{\Delta f_d, \theta \to 0} \tilde{S}(\Delta f_d, \theta)$$

=
$$\lim_{\Delta f_d, \theta \to 0} D \frac{\sin(\pi \Delta f_d T)}{\pi \Delta f_d} e^{j(\theta + \pi \Delta f_d T)}$$

= $\pm D$

- (18) Code-phase Delay: Once the tracking loop has been locked, the signal samples can be delayed by the amount of code-phase offset so that the packet samples coincide exactly with chips and hence navigation bits. The processor uses this delay information to compute psuedo-range finely.
- (19) Tracking Switch: The switch controls initiation of the tracking loop. Once tracking has started, the processor can switch from tracking to acquisition if a loss of lock is detected
- (20) A common counter: The counter maintains milisecond count. The processor can keep a record of the counter along with the Nav bits to compute coarse psuedorange based on time differences for different satellites
- (21) The Processor: Handles high level tasks of PVT computation and controlling the corelator co-processor

- (22) The PRN code generator: The receiver may have the shift register setup to dynamically generate the PRN codes in the corelator block or processor can have a look-up table for the same.
- (23) Intermediate Frequency: The Processor should set f_i to be used by the system.